

JEDEC STANDARD

Power MOSFET Equivalent Series Gate Resistance Test Method

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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**POWER MOSFET EQUIVALENT SERIES
GATE RESISTANCE TEST METHOD**

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POWER MOSFET EQUIVALENT SERIES GATE RESISTANCE TEST METHOD

(From JEDEC Council Ballot JCB-96-21, formulated under the cognizance of JC-25 Committee on Transistors.)

1 Purpose

This test method provides a means of qualitatively estimating power MOSFET high speed switching gate propagation effects. In conjunction with gate charge measurements (JESD24-2), it can adequately assess the switching capability of a power MOSFET device. ESR and gate charge tests, together, provide an alternative to high speed, high current switching measurements where test circuit stray impedances mask device characteristics. The tests are best implemented by the device manufacturer to ensure switching consistency for the users in their circuit.

2 Keywords

Transistor
Power MOSFET
Test
Measurement
ESR
Gate resistance
Gate charge
Switching speed

3 Scope

The measurement outlined in this document is intended for power MOSFET devices, n- or p-type.

4 Background

Differences in test circuit wiring have been the root cause for industry's inability to reach agreement on high speed switching measurements. Switching time round robins conducted by the JEDEC JC-25 Committee on Transistors has highlighted the inability to reach reasonable agreement when measuring identical devices. Measurements presented to JC-25 have shown that the test socket itself can be a major factor in the perceived switching performance. These difficulties have prompted this alternative. ESR reflects changes in die gate processing, e.g., contact resistance, metalization, and polysilicon doping level, all of which affect high speed performance. A process fault usually results in an ESR increase of an order of magnitude or more.

5 Symbols, terms, and definitions

V_{DS}	Drain-source dc bias voltage
f	Test frequency
ESR	The lumped parameter device resistance in series with the device gate-source capacitance.
C_{GS}	The gate-source capacitance measured with the drain open circuited.
C_{iss}	The MOSFET input capacitance with drain-source ac shorted.
T_j	Junction temperature

6 Test and requirements

The measurement can be made with an LCR meter of which there are many commercially available. A test frequency that gives a capacitive reactance of $<1000 \Omega$ for an ESR $<10 \Omega$ should lead to reasonable test results. A small die (4 mm^2) will need a higher test frequency than a large die (60 mm^2) to maximize the phase shift for a more repeatable measurement. In general an ESR reading does not change with a two-terminal (C_{GS}) or three-terminal (C_{iss} with or without a V_{DS}) test. A high test frequency, optimized for ESR, can lower a C_{iss} value because of socket and device inductance if ESR is obtained in conjunction with a three-terminal C_{iss} measurement. A two-terminal test is preferred. The following should be specified: T_j , V_{DS} , f , and circuit type. ESR is the measured parameter.

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